Claims

I claim:

1. A circuit comprising:

a signal input to receive a signal;

a buffer circuit to receive the signal input and to generate a buffer circuit output; and

a voltage following circuit to receive the signal input and to generate a voltage following output wherein the buffer circuit output and the voltage following circuit output are coupled to a circuit output node.

2. The circuit of claim 1 wherein the voltage following circuit comprises a first amplifier, including a positive input, a negative input and an output, and, a NMOS transistor including a gate, a source and a drain,

the positive input of the first amplifier being coupled to receive the input signal, the negative input of the first amplifier being coupled to the source of the NMOS transistor, the output of the first amplifier being coupled to the gate of the NMOS transistor, the drain of the NMOS transistor being coupled to a positive supply voltage, and the source of the NMOS transistor being coupled to the circuit output node, and

a second amplifier, including a positive input, a negative input and an output, and, a PMOS transistor, including a gate, a source and a drain, the positive input of the second amplifier being coupled to receive the input signal, the negative input of the second amplifier being coupled to the source of the PMOS transistor, the output of the second amplifier being coupled to the gate of the PMOS transistor, the drain of the PMOS transistor being coupled to a supply voltage less than the positive supply voltage, and the source of the PMOS transistor being coupled to the circuit output node.

3. The circuit of claim 2 wherein the positive input of the first amplifier is coupled to the signal input through a first output level based buffer impedance modulator circuit and the positive input of the second amplifier is coupled to the signal input through a second output level based buffer impedance modulator circuit.

4. The circuit of claim 1 wherein the voltage following circuit comprises a NMOS transistor including a gate, a source and a drain, the gate being coupled to receive the input signal, the drain being coupled to a positive supply voltage, and the source being coupled to the circuit output node, and

a PMOS transistor including a gate, a source and a drain, the gate being coupled to receive the input signal, the drain being coupled to a supply voltage less than the positive supply voltage, and the source being coupled to the source of the NMOS transistor and the circuit output node.

5. The circuit of claim 1 wherein the buffer circuit comprises a first inverter including an input coupled to receive the input signal and an output, and

a second inverter including an input coupled to the output of the first inverter and an output coupled to the circuit output node.

6. The circuit of claim 1 wherein the circuit is part of a signal distribution system.

7. The circuit of claim 6 wherein the circuit is a repeater circuit in a signal distribution system.

8. The circuit of claim 6 wherein the circuit is a buffer circuit at a distribution junction of the signal distribution system.

9. The circuit of claim 1 wherein the circuit is part of a large scale integrated circuit.

10. The circuit of claim 1 wherein the signal input comprises a resistive termination.

11. A method of buffering an input signal comprising:

receiving the input signal;

generating an output signal to follow the voltage of the input signal;

generating a buffered signal; and

coupling the buffered signal to the output signal to generate a buffered output signal.

12. The method of claim 13 wherein generating the output signal comprises

generating a high output signal when the input signal is high, and

generating a low output signal when the input signal is low.

13. The method of claim 12 wherein generating the high output signal includes generating the high output signal substantially independent of power supply noise and generating the low output signal substantially independent of power supply noise.

14. The method of claim 11 wherein generating the buffered signal comprises

inverting the signal to generate an intermediate signal; and

inverting the intermediate signal to generate the buffered signal.

15. A means for buffering an input signal comprising:

means for receiving the input signal;

means for generating a output signal to follow the voltage of the input signal;

means for generating a buffered signal; and

means for coupling the buffered signal to the voltage following output signal to generate a buffered output signal.

16. The means of claim 15 wherein the means for generating a voltage following output signal comprises

means for generating a high output signal when the input signal is high, and

means for generating a low output signal when the signal is low.

17. The means of claim 16 wherein the means for generating the high output signal comprises means for generating a high output signal substantially independent of power supply noise and the means for generating the low output signal comprises means for generating a low output signal substantially independent of power supply noise.

18. The means of claim 15 wherein the means for generating the buffered signal comprises

means for inverting the signal to generate an intermediate signal; and

means for inverting the intermediate signal to generate the buffered signal.

19. A system comprising:

a microprocessor comprising a circuit including

a signal input to receive a signal;

a buffer circuit to receive the signal input and to generate a buffer circuit output; and

a voltage following circuit to receive the signal input and to generate a voltage following output wherein the buffer circuit output and the voltage following circuit output are coupled to a circuit output node.

20. The system of claim 19 wherein the voltage following circuit comprises a first amplifier, including a positive input, a negative input and an output, and, a NMOS transistor including a gate, a source and a drain,

the positive input of the first amplifier being coupled to receive the input signal, the negative input of the first amplifier being coupled to the source of the NMOS transistor, the output of the first amplifier being coupled to the gate of the NMOS transistor, the drain of the NMOS transistor being coupled to a positive supply voltage, and the source of the NMOS transistor being coupled to the circuit output node, and

a second amplifier, including a positive input, a negative input and an output, and, a PMOS transistor, including a gate, a source and a drain, the positive input of the second amplifier being coupled to receive the input signal, the negative input of the second amplifier being coupled to the source of the PMOS transistor, the output of the second amplifier being coupled to the gate of the PMOS transistor, the drain of the PMOS transistor being coupled to a supply voltage less than the positive supply voltage, and the source of the PMOS transistor being coupled to the circuit output node.

21. The circuit of claim 19 wherein the voltage following circuit comprises a NMOS transistor including a gate, a source and a drain, the gate being coupled to receive the input signal, the drain being coupled to a positive supply voltage, and the source being coupled to the circuit output node, and

a PMOS transistor including a gate, a source and a drain, the gate being coupled to receive the input signal, the drain being coupled to a supply voltage less than the positive

supply voltage, and the source being coupled to the source of the NMOS transistor and the circuit output node.

22. A machine-readable medium having stored thereon instructions, which when executed by a set of processors, cause said set of processors to perform the following:

receive an input signal;

generate an output signal to follow the voltage of the input signal;

generate a buffered signal; and

couple the buffered signal to the output signal to generate a buffered output signal.

23. The machine readable medium of claim 22 wherein the instructions to generate an output signal comprise instructions to

generate a high output signal when the input signal is high, and

generate a low output signal when the input signal is low.

24. The machine readable medium of claim 23 wherein instructions to generate the high output signal includes instructions to generate the high output signal substantially independent of power supply noise and wherein the instructions to generate the low output signal includes instructions to generate the low output signal substantially independent of power supply noise.

25. The machine readable medium of claim 22 wherein the instructions to generate the buffered signal comprise instructions to

invert the input signal to produce an intermediate signal; and

invert the intermediate signal to generate the buffered signal.